

Abstract

The present invention provides a margin testing system, incorporated in an electronic system (e.g., a computer system), that includes a controller, a frequency control module, and a voltage control module, and a fault bypass module. In response to commands from the controller, the frequency control module and/or the voltage control module can set a test clock frequency and/or a test voltage for application to one or more components of the electronic system to elicit system response to these test values. The response of the system at each test value can be monitored, e.g., by executing a diagnostics software, and analyzed. The fault bypass module can mask fault signals during margin testing to ensure that these signals will not disrupt margin testing of the system.

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